Computational Sciences and Engineering 2(2) (2022) 211-216

University of Guilan

Computational Sciences and Engineering

journal homepage: https://cse.guilan.ac.ir/

Novel Drain Recessed Oxide SOI-MOSFET For Reduction of Short-Channel-Effects

Mohammad K. Anvarifard *

Department of Engineering Sciences, Faculty of Technology and Engineering, East of Guilan, University of Guilan, Rudsar-Vajargah, Iran.

ARTICLE INFO

Article history:
Received 02 January 2023
Received in revised form 05 February 2023
Accepted 07 February 2023
Available online 07 February 2023

Keywords:
SOI-MOSFET
Short channel effect
Threshold voltage
Recessed oxide

ABSTRACT

Since the device performance is degraded with the elapsed time, it is essential to develop the novel device for enhancing the reliability. Hence, a modification inside the drain region of the SOI-MOSFET structure has been performed. A region oxide has been recessed in the drain in order to modify the electric field owing to dielectric permittivity change. The simulation results obtained by SILVACO showed the improvement of the short-channel effects in the terms of drain-induced barrier lowering, hot-carrier effects and threshold voltage fluctuation as compared to the conventional structure.

1. Introduction

The study of the nanoscale devices is vital owing to high density of integrated circuits. But with leading devices to nanoscale limit, the descriptive effects such as hot carrier effect (HCE), high off current and high gate current are explored. There are many reasons why the silicon-on-insulator (SOI) technology is one of the solutions in nanoscale structures can be mentioned as lower short channel effects (SCEs), excellent latchup immunity, higher drive current, and reduced junction capacitances [1].

Many works have been performed for performance improvement of SOI MOSFETs with respect to their counterpart i.e. conventional SOI MOSFET in suppressing SCEs. A novel configuration for the double gate (DG) SOI MOSFET using two side gates has been presented in order to reducing SCEs [2]. The asymmetrical DG SOI MOSFET with n^+ and p^+ polysilicon gates for higher drive current has been investigated and shown is superior to symmetrical DG counterparts [3]. An

* Corresponding author.
E-mail addresses: m.anvarifard@guilan.ac.ir

https://doi.org/10.22124/cse.2023.23783.1045

asymmetric Schottky tunneling source MOSFET utilizing the concept of gate-controlled Schottky barrier tunneling has been presented and demonstrated [4].One study has been done to investigate the effects of substrate orientation and longitudinal channel stress on the performance of extremely thin SOI MOSFET [5-8].

In this work, a new structure of SOI-MOSFETs with excellent performance is proposed. The goal of the present work is to state the unique features exhibited by a novel nanoscale asymmetrical SOI-MOSFET in which the drain active layer consists of a recessed insulator region made of SiO2.

This paper focuses on the improvement of the SCEs. The proposed structure has been compared to the conventional SOI MOSFET (C-SOI). Utilizing two-dimensional simulator [9], the undesirable effects such as hot carrier effect, off current, gate current and DIBL of proposed structure is disappeared thus making it a more reliable device configuration than the C-SOI MOSFET for high performance CMOS circuit applications.

2. Device Structure

Fig. 1 has illustrated a perspective of the proposed device including a recessed oxide inside the drain region. The recessed oxide is described by the variable RO which is 2 nm in this work. The RO is made of the SiO_2. For this reason, the suggested device is named as RO-SOI MOSFET.

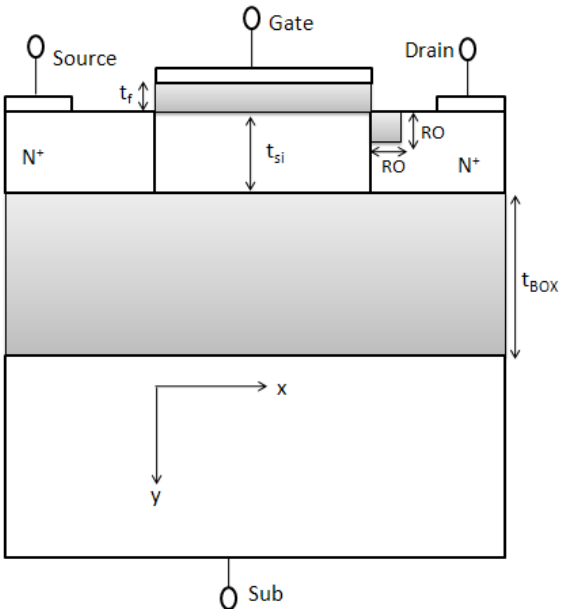

Figure 1. A cross-sectional view of the proposed device.

All parameter values of C-SOI are equal to proposed device parameters unless otherwise stated. The typical parameter values have been selected according to road map of semiconductor technology [10]. It is worth noting that the quantum moments model is implemented for simulation of structures. The typical parameters for the device simulation have been given at the table 1.

Table 1. The typical parameters of the proposed structure.

Parameter	Value
Channel length	32 nm
Gate oxide thickness, t_f	1 nm
Buried oxide thickness, t_{BOX}	100 nm
RO	2 nm

3. Results

Fig. 2 shows the output characteristics of the devices under the study. One of the mind parameters in devices is their drive currents. As shown as the figure, the drain current of the proposed device is equal to the drain current of its counterpart i.e. C- SOI. Therefore, we can compare the suggested device and the C-SOI structure in identical drain currents.

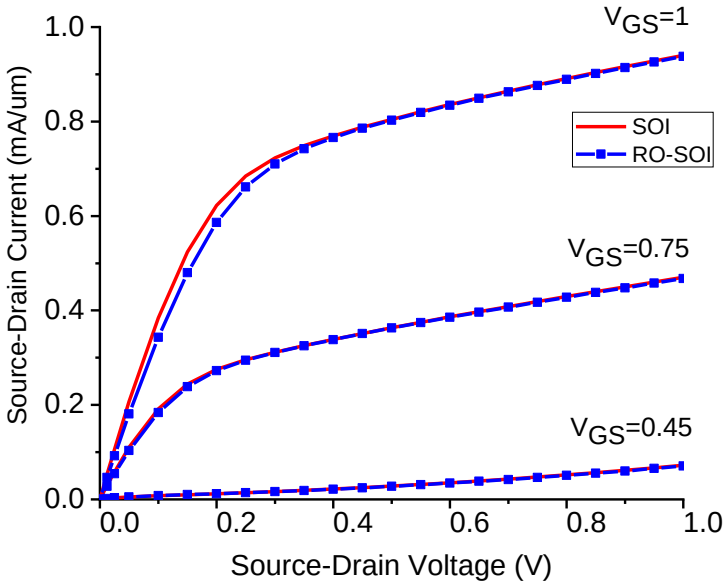

Figure 2. The drain current as a function of the drain voltage for the structures.

The reduced electric field reduces the trap in the gate oxide and improves the hot carrier effects. The surface electric field along the channel has been illustrated for the RO-SOI and the C-SOI structures in Fig. 3. As shown in the figure the electric field of IR-SOI inside the drain region is considerably less than that the C-SOI. Indeed, the recessed insulator region causes the electric field redistributed along the channel. Therefore, with stated evidences above, the hot carrier effect improves in the RO-SOI structure.

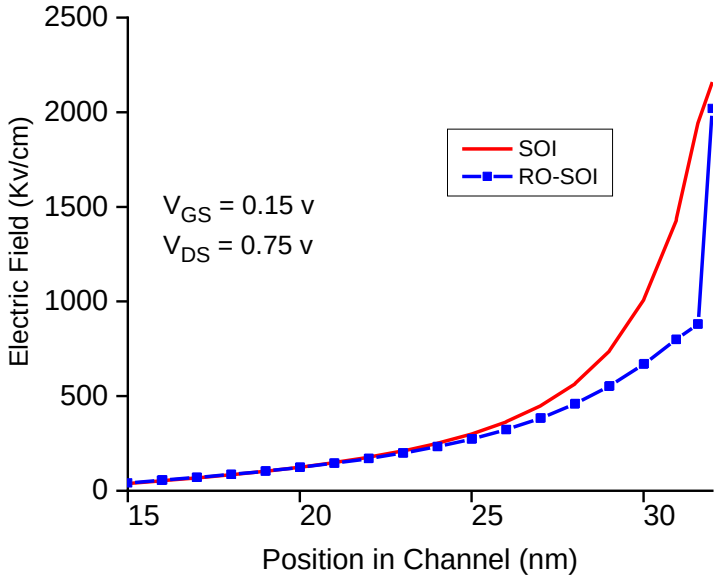

Figure 3. Electric field profile along the surface of channel for the RO-SOI and C-SOI structures.

Fig. 4 shows the dependence of the threshold voltage on the channel length. As can be seen from the figure the RO-SOI obtains a lower threshold voltage which is very good in scaling aims.

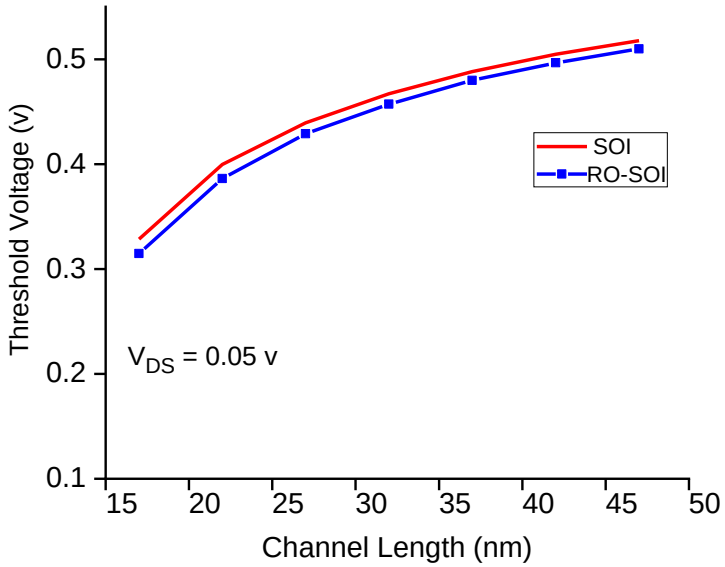

Figure 4. The threshold voltage upon the channel lengths for the RO-SOI and C-SOI structures.

The DIBL which is as result of nonuniform charge distribution in the channel has been investigated for the devices under the study. Indeed, this variable shows the effect of the drain voltage on the threshold voltage. In Fig. 5, the DIBL of devices has been demonstrated.

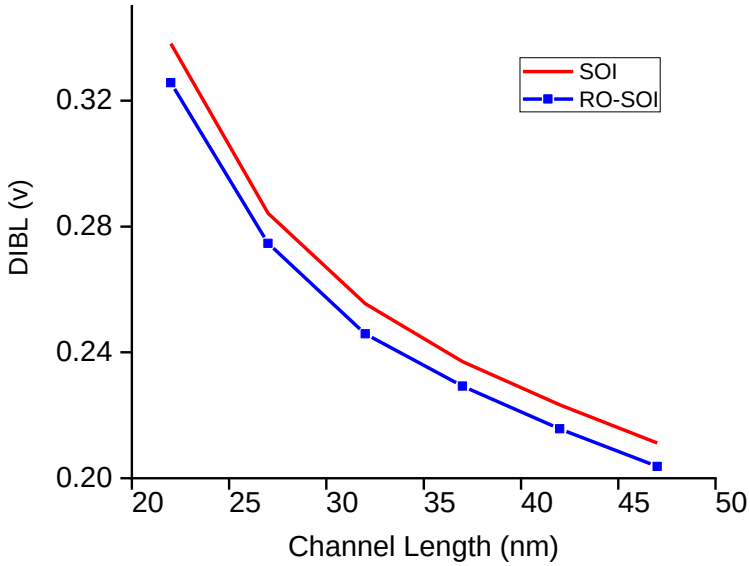

Figure 5. The DIBL upon the channel lengths for the RO-SOI and C-SOI structures.

As shown in the figure, the DIBL of the RO-SOI is less than that of the C-SOI which is very desirable.

The silicon layer thickness can affect the threshold voltage. For this reason, the threshold voltage as a function of the silicon layer thickness has been plotted in Fig. 6. It can be seen from the figure that the variation rate for the RO-SOI is less than that for the C-SOI which is very desirable. It is worth noting that fully depleted SOI is sensitive to the silicon layer thickness and the reduction of this sensitivity is important.

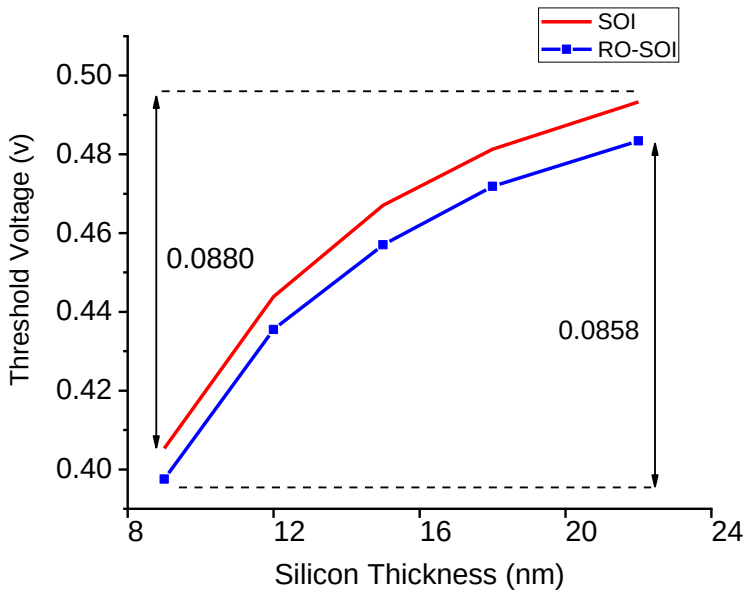

Figure 6. The threshold voltage upon the silicon thickness for the RO-SOI and C-SOI structures.

Fig. 7 shows the off current as a function of the channel length in the logarithmic scale for the RO-SOI and C-SOI structures. It can be seen from the figure that the off current of RO-SOI structure is less than that in the C-SOI structure. Therefore, the RO-SOI has lower dissipation power in comparison with the C-SOI at standby mode.

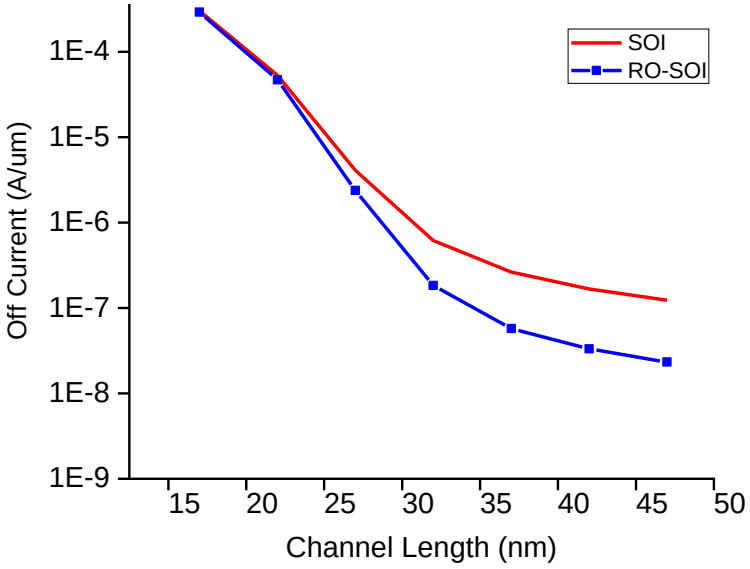

Figure 7. Off current versus channel length for the RO-SOI and the C-SOI structures.

In the small signal applications, it is essential to reduce gate current. Also, the hot electron reliability can be investigated by the gate current. Since the lower gate current shows the higher input impedance, then the amplification rate increases. Also, the reduction of the gate current shows lower degradation mechanism. In Fig. 8 the gate current versus the channel length in logarithmic scale for the RO-SOI and C-SOI structures have been illustrated. It can be seen from the figure that gate current of RO-SOI is less than the gate current of C-SOI. Therefore, the input resistance of RO-SOI structure is higher.

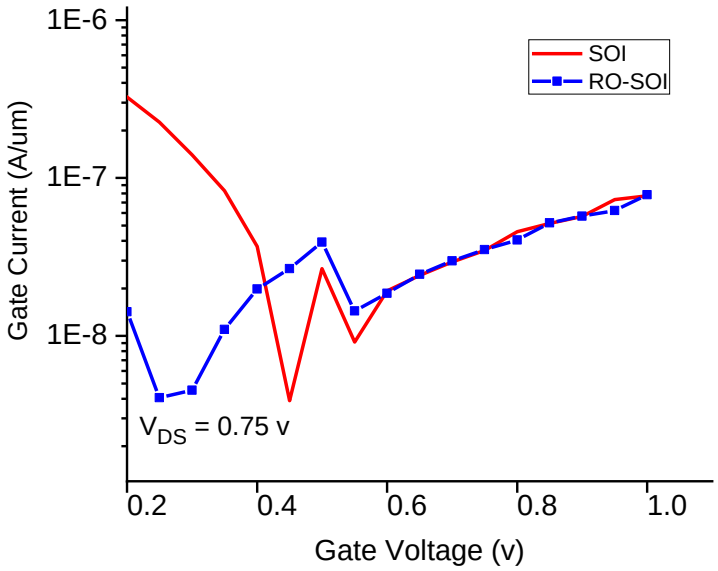

Figure 8. Gate current versus the gate voltages for the IR-SOI and C-SOI structures.

3. Conclusions

With inserting an extra oxide (SiO_2) inside the Drain region of a fully depleted SOI, the electric field is redistributed and reduced in the drain. The reduction of the electric filed is caused by the dielectric permittivity change in the device owing to recessed oxide for the proposed device. The RO has been selected as 2 nm in this work. Regarding the idea proposed in this work, the important parameters in the cases of DIB, off current, gate current and HCE have been improved in the RO-SOI. The comparison of these obtained results between the RO-SOI and the conventional C-SOI structure shows that the proposed structure can be one proper substitution for the C-SOI structure.

References

[1] T. Ohno, Y. Kado, M. Harada, T. Tsuchiya, IEEE Transaction on Electron Devices 42 (1995) 1481–1486.
[2] A. A. Orouji, M. J. Kumar, MicroelectronicEngineering 83 (2006) 409-414.
[3] K. Kim, J. G. Fossum, IEEE Transaction on Electron Devices48 (2001) 294-299.
[4] R. Jhaveri, V. Nagavarapu, J. C. S. Woo, IEEE Transaction on Electron Devices56 (2009) 93-99.
[5] A.Majumdar, C. Ouyang, S. J. Koester, W. Haensch, IEEE Transaction on Electron Devices 57 (2010) 2067-2072.
[6] Z. Ramezani and A. A. Orouji, "Investigation of veritcal graded channel doping in nanoscale fully-depleted SOI-MOSFET," *Superlattices and Microstructures*, vol. 98, pp. 359-370, 2016.
[7] P. Vimala and C. Usha, "Modeling of Source Pocket Engineered PNPN Tunnel FET on High-K Buried Oxide (H-BOX) Substrate for Improved ON Current," *Silicon*, pp. 1-7, 2022.
[8] S. Singh, A. Sharma, V. Kumar, P. Umar, A. K. Rao, and A. K. Singh, "Investigation of N+ SiGe juntionless vertical TFET with gate stack for gas sensing application," *Applied Physics A*, vol. 127, no. 9, pp. 1-11, 2021.
[9] International device simulation software, SILVACO TCAD, 2010.
[10] International technology roadmap for semiconductor. Availablefromhttp://public.itrs.net.