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Novel CNTFET with negative/positive slope impurity distribution to manage the nano-dimension effects

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ABSTRACT

Where a transistor is scaled to the nano dimension, it faces the problem of short-channel effects (SCEs), which reduce the gate control over the channel. The operation of carbon nanotube field effect transistors (CNTFETs) is completely sensitive to SCEs. Here, we propose a specific doping profile to manage the SCEs in CNTFETs. It includes graded doping with negative or positive slope for different regions of device. This profile manages the band to band tunneling and boosts the current ratio, subthreshold swing, and voltage gain. Tus, the proposed device is a transistor with improved short channel characteristics. Numerical simulation is used to obtain the results from Poisson and Schrodinger equations.

1. Introduction

By scaling the transistors, the number of devices on chip are increased and it brings the transistors closer to short channel and quantum confinements. It creates a series of challenges and limitations such as augmentation of tunneling and leakage currents, considerable power dissipation and higher thermal degeneracy, difficulties in lithography-based techniques, rising in cost of production, and etc. Therefore, new transistors or new structures must be proposed in order to reduce these challenges as much as possible [1].

Carbon nanotubes (CNTs) are composed of a long chain of its own atoms called catenation [2]. They are strong competitor because of their outstanding mechanical, electronic, and thermal properties [3]. One of the most important features of CNT is that it can act as a semiconductor or as a metal [2,4]. The bandgap in semiconductor carbon nanotubes decreases with increasing

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diameter [5]. Short-channel effects (SCEs), such as drain induced barrier lowering (DIBL), leakage current, punch through, etc, reduce the performance of the transistors [6]. Using CNT, the device performance is improved compared to conventional MOSFETs [7].

CNT field effect transistors (CNTFETs) have been studied by scientists due to their scalability and gate controllability [8]. CNTFETs show proper mobility of carriers, conduction in ballistic regime and brilliant switching behavior, but may they include unwanted behaviors such as low saturation current, high gate-source capacitance, and ambipolar behavior [7,9]. To overcome the deficiencies of electronics devices and using their benefits, proposing the modified structures is a advantageous strategy [10,11]. Researchers have analyzed these devices and proposed different modified structures to be used in different aspects of electronics and communication engineering [12-15]. In [16] a doping-less structure with proper digital and analog outputs was presented to omit the doped reservoirs. In [17] using the hybrid combination of electrically junction and step doping was employed to enhance the CNTFET outputs. Also, in [18], the effects of Gaussian doping profile was examined and its results were analyzed. In [19], different gate metals are applied to increase the current capability of these devices.

In this paper, a novel CNTFET with negative/positive slope impurity distribution is proposed to manage the undesired nano-dimension effects. The impurity distribution is engineered for all three main sections of device including gate, drain, and source to lower the SCEs. The slope of impurity distribution is positive or negative depending on required control on carriers transform. Numerical simulation is done using Poisson and Schrodinger equations based on self-consistent method and None-Equilibrium Green's Function. Quantum effects in nano dimension regime are considered by mentioned equations and methods. The results demonstrate that by applying this novel structure the device show better current ratio, SS, DIBL, and voltage gain compared with conventional CNTFET (C-CNTFET).

2. Device structure

Figure 1 illustrates the device and its proposed doping profile distribution. The device contains of a zigzag (17,0) carbon nanotube with a diameter of 2.6 nm, considering the following distribution of doping for gate, source and drain where the maximum level of impurity is 1 nm^{-1}. Here the doping density is applied linearly at gate, drain and source. In this way, firstly, the doping in the source part is maximum and as it gets closer to the gate, it is reduced to zero (the absolute value of doping apart from P or N type). In the gate section, the doping is initially considered high and as it gets closer to the drain, the doping decreases gradually. The drain part distribution is the opposite of gate and source, i.e. the doping starts from zero and increases gradually. By this arrangement of doping distribution, it increases the horizontal difference between the valence band and conduction bands at junctions, which reduces tunneling. When the tunneling decreases, it causes to reduce the leakage current. When impurities increase at the two end edges of the drain and the source, the Schottky barrier will be diminished effectively. A gate is located around the nanotube channel region separated by an oxide (HfO_2) as the dielectric coating. This layer has 2 nm depth and a dielectric constant of 16. This device works at a temperature 300°K. Channel length is 10 nm and drain and source length is 30 nm. It should be mentioned that in conventional structure, the source/drain doping is fixed at 1 nm^{-1} and channel is intrinsic. Other parameters and dimensions of both structures are the same.

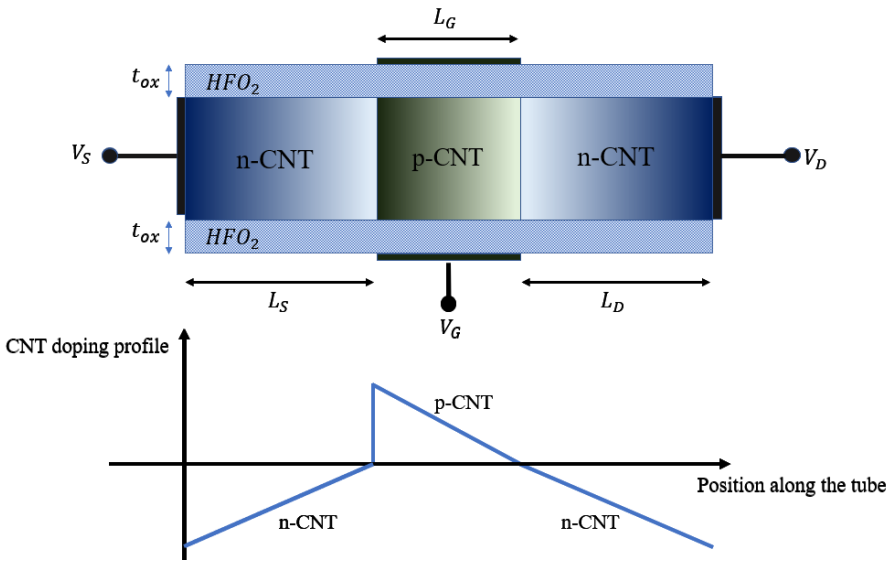

Figure. 1. New structure of CNTFET at the doping distribution at each region to manage the BTBT.

3. Simulation method and results

The Poisson equation is obtained from the following relation [17] with the discretization of 0.2 nm in each direction:

$$\frac{\partial^2 u_j(r.z)}{\partial r^2} + \frac{1}{r}\frac{\partial u_j(r.z)}{\partial r} + \frac{\partial^2 u_j(r.z)}{\partial z} = \frac{-q}{\varepsilon} p(r.z) \qquad (1)$$

The relationship between charge density distribution is shown below [16]:

$$p = \left(r = r_{CNT}.z_j\right) = p\left(z_j\right) - n\left(z_j\right) + N_D^+ - N_A^- \qquad (2)$$

$$p \neq (r = r_{CNT}.z) = 0 \qquad (3)$$

r is radius and z is one dimension of CNT without symmetry. N_D is donor density and N_A is acceptor density. The transfer factor is stated by the Green function:

$$G_q(E) = \left[(E + i\eta^+)I - H - \sum_S - \sum_D \right]^{-1} \qquad (4)$$

where η^+ is a tiny positive worth, Σ_S and Σ_D are the self-energies of the source(S)/drain(D), H is the Hamiltonian matrix in nanotube, energy is E, and the identity matrix is denoted by I, respectively. The Hamilton matrix mode space has been selected to speed up the device simulation. The Hamilton matrix is presented as follows [19]:

$$H = \begin{bmatrix} U_1 & b_{2q} & & & & \\ b_{2q} & U_2 & t & & & \\ & t & U_3 & b_{2q} & & \\ & & b_{2q} & U_4 & \ddots & \\ & & & \ddots & \ddots & b_{2q} \\ & & & & b_{2q} & U_N \end{bmatrix}_{N\times N} \qquad (5)$$

The following equation can be solved analytically and finally the energy obtained from the source can be calculated from the equation [17]:

$$\sum_{S}(1,1) = \frac{(E-U_1)^2 + t^2 + b_{2q}^2 \pm \sqrt{\left[(E-U_1)^2 + t^2 + b_{2q}^2\right] - 4(E-U_1)^2 t^2}}{2(E-U_1)} \quad (6)$$

The current for different bias conditions (GS and GD voltages) are considered from the following equation [16]:

$$I = \frac{2q}{h}\int T(E)\,[F(E-E_{FS}) - F(E-E_{FD})]dE \quad (7)$$

where q is the charge of electron, E_{FS} and E_{FD} are the Fermi level of the S and D, the Planck constant is denoted by h, and the transfer coefficient is T (E) considered as follows:

$$\mathrm{T(E)} = \mathrm{trace}(\Gamma_S \mathrm{G}\,\Gamma_D \mathrm{G}^{+}) \quad (8)$$

where Green's function is G, and $\Gamma_{s(D)}$ is the energy level expansion because of S and D connections, calculated by the subsequent equation:

$$\Gamma_{S(D)} = i(\sum_{SD} - \sum_{SD}^{+}) \quad (9)$$

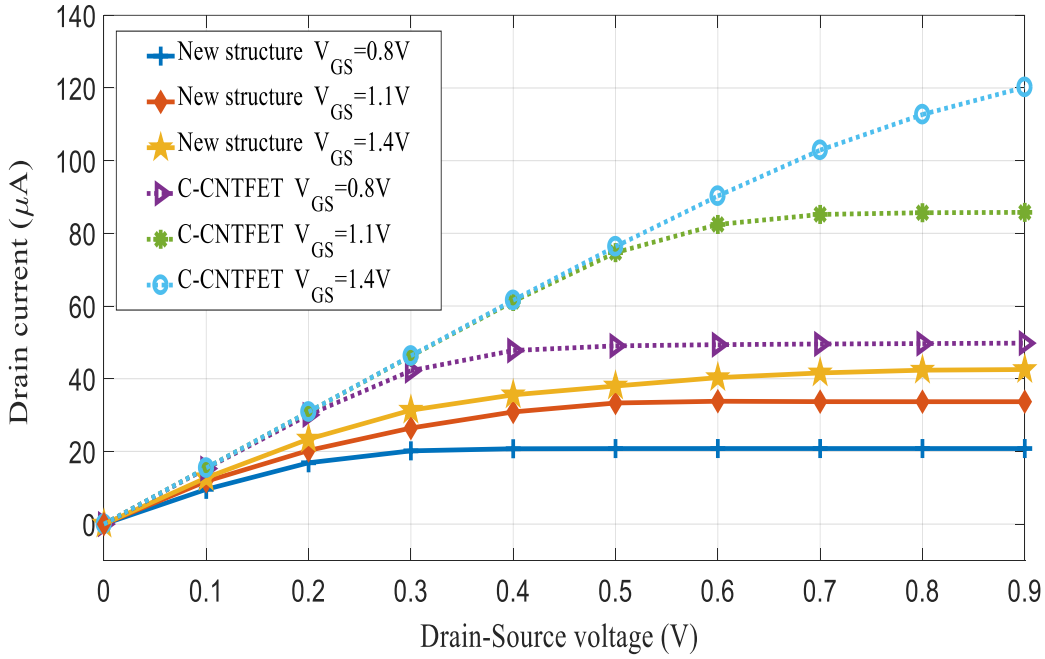

Figure 2. I_D versus V_D in terms V_{GS} = 0.8, 1.1, and 1.4 V where L_G = 10 nm for new and conventional devices

Using the above method, here the results of numerical simulations are mentioned. As illustrated in ***Figure 2***, the transistor current for the new and the C-CNTFET structures are compared. It reveals that the saturation current is higher in C-CNTFETs which is the direct result of using p-type doping in the channel in proposed structure. Here three different voltages, V_{GS} = 0.8 V, V_{GS} = 1.1 V and V_{GS} = 1.4 V are investigated for both structures.

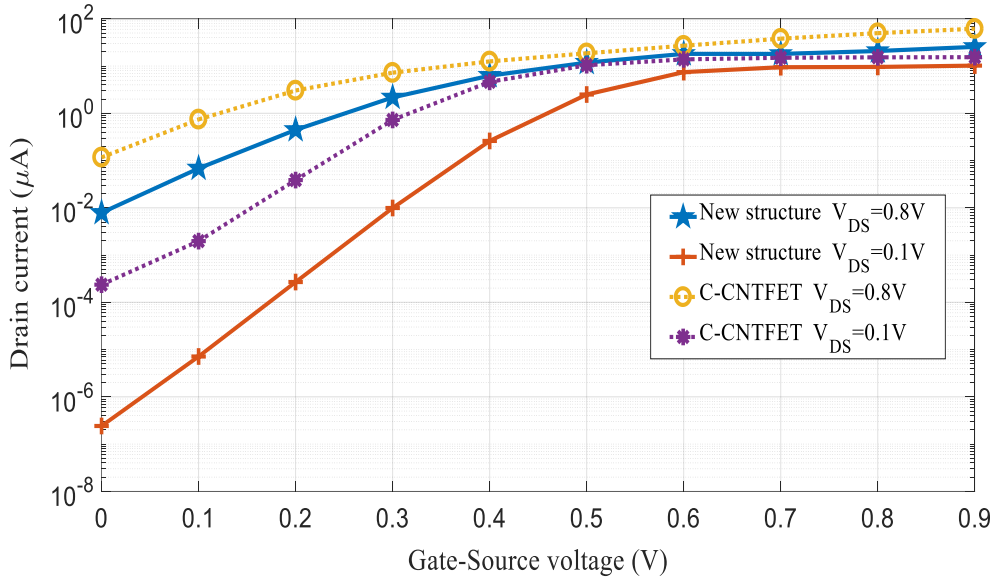

Figure 3. I_D diagram versus GS voltage for new and C-CNTFET structures at V_{DS} = 0.1, and 0.8 V and L_G = 10 nm.

Figure 3 shows the features of the I_D in terms of GS voltage with different V_D for both structures. The novel structure considerably reduces the leakage current. From ***Figures 2 and 3***, it is concluded that the novel device results in lower saturation current but much lower leakage current. This means enhancement in current ratio by applying the novel structure. The lessening in leakage current is due to the linear outline of impurity which rises the horizontal distance between conduction and valance bands at channel to drain junction which sequentially weakens the possibility of band to band tunneling (BTBT).

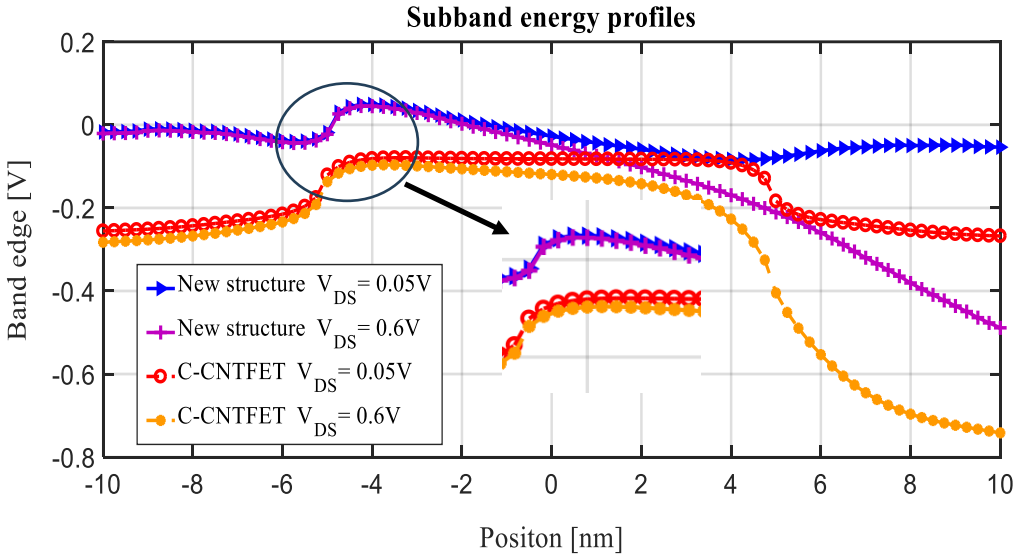

Figure 4. Diagram of potential distribution along the nanotube length for new structure and C-CNTFET at V_{DS} = 0.05, 0.6 V And V_{GS} = 0.5 V.

DIBL means reduction in channel barrier by change in V_{DS}. ***Figure 4*** investigates the DIBL for both devices. The drain voltage is changed from 0.05 to 0.6. The energy band diagram at source to channel junction shows the barrier. As can be observed, the novel structure effectively reduces the DIBL which is one of the main issues for nano dimension devices. Its relation is as follows:

$$DIBL = \frac{V_{TH}(lowV_{DS}) - (V_{TH}(highV_{DS})}{highV_{DS} - lowV_{DS}} \quad (10)$$

Where V_{TH} is threshold voltage.

Figure 5, 6, and 7 show and compare ON, OFF, and ON/OFF ratio currents in terms of channel length for the new and conventional structures at voltage V_{GS} = 0.8 V, V_{DS} = 0.8 V for ON current and V_{GS} = 0.0 V, V_{DS} = 0.8 V for OFF current. As mentioned before, due to the suppressed OFF current in proposed device, it results in substantial enhancement in current ratio.

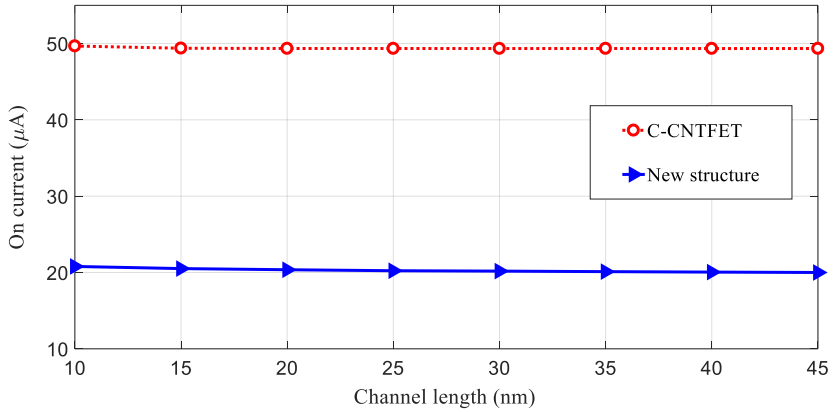

Figure 5. Saturation current variation by channel length while the bias is fixed at V_{GS} = 0.8 V, V_{DS} = 0.8 V.

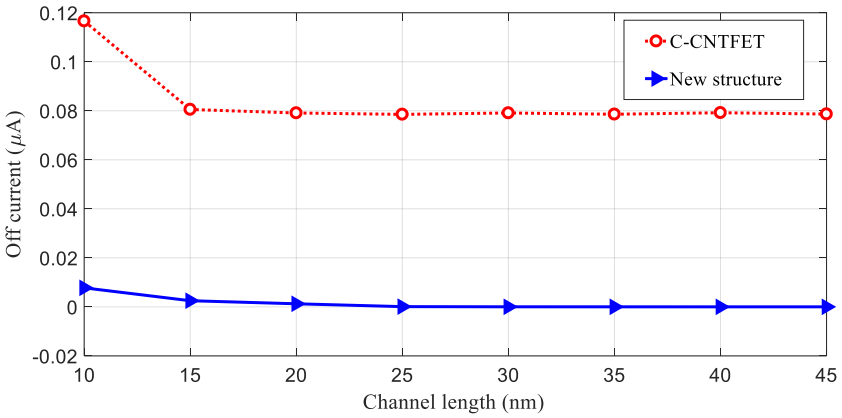

Figure 6. Leakage current variation by channel length while the bias is fixed at V_{GS} = 0.0 V, V_{DS} = 0.8 V.

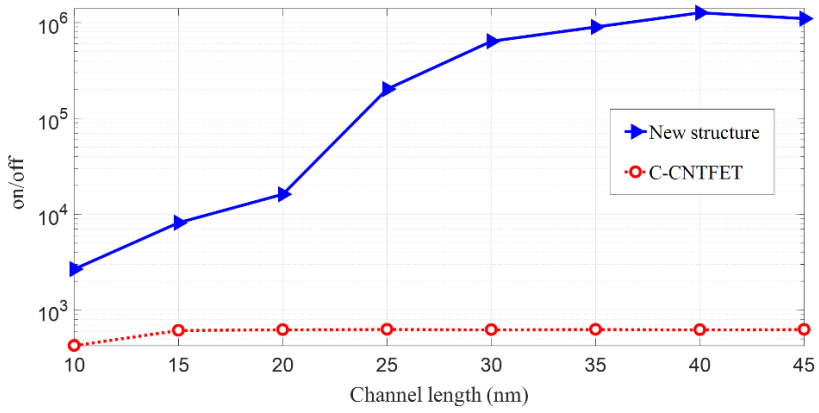

Figure 7. ON/OFF current ratio variations by channel length while the bias is fixed at V_{DS} = 0.8 V.

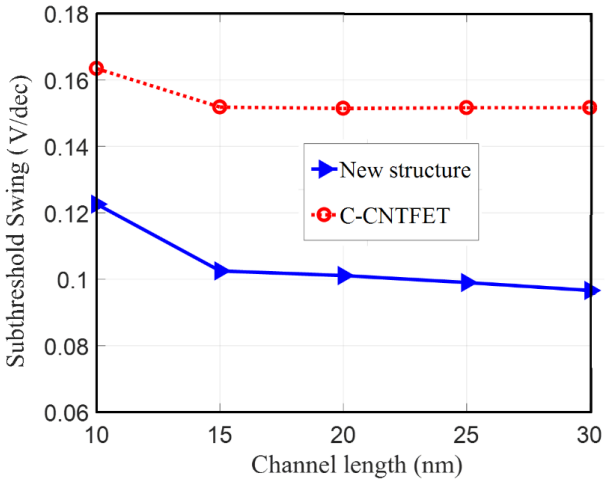

Figure 8. The SS diagram in terms of channel length for the new structure and C-CNTFET

In nano transistors, proportional to V_G, the minority carriers depend on surface voltage. In low voltages this issue determines the subthreshold behavior of the device. Smaller subthreshold swing (SS) means lower power dissipation at OFF state. The relation for SS is as follows:

$$SS = \frac{dV_{GS}}{dlogI_{DS}} \tag{11}$$

Figure 8 illustrates the SS drawing in terms of channel length for both structures. As seen, in 20 nm length, the SS is reduced from about 156 mV/dec to 100 mV/dec. This figure reveals that the SS for the nonuniform impurity spreading of the channel is reduced compared to the conventional structure which demonstrates another benefit for this engineered structure.

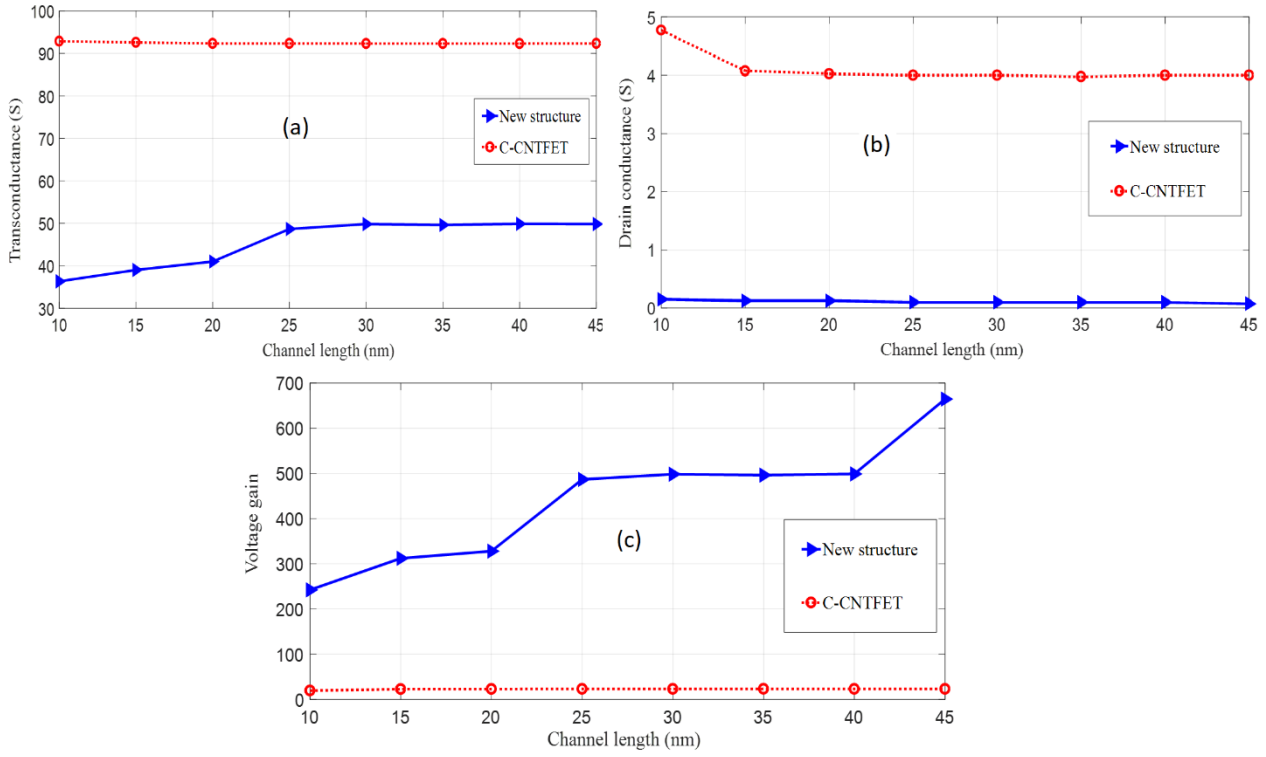

Figure 9. (a) Transconductance (b) drain- conductance and (c) the voltage gain diagram in terms of channel length for new structure and C-CNTFET

Figure 9 shows the voltage gain (g_m/g_d) which is the ratio of transconductance to drain-conductance. It indicates considerable higher values for the new structure. It is directly the outcome of a small drain-conductance of proposed device which outperforms the reduction in its transconductance.

4. Conclusion

Similar to other nano dimension transistors, CNTFETs suffer from SCEs. This issue can be controlled by applying new structures. In this report, doping distribution is done with negative and positive slope in G, D and S regions of CNTFETs. To achieve the results, numerical assessment of Schrodinger and Poisson equations has been done. This controls the BTBT in junctions and consequently improves the leakage flow, DIBL, and SS. Also, the voltage gain experiences significant enhancement by applying this doping profile. It is concluded that the negative and positive expansion of impurity will effectively manages the SCEs in CNTFETs and the proposed structure is a proper candidate for both digital and analog applications.

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